

undershooting of the desired magnitude ( $U_{OL}$ ) by the actual  
5 magnitude ( $U_{Mess}$ ).

Q9 4. (Amended) The drive circuit as claimed in claim 1,  
characterized in that it comprises a monitoring unit (50, 50b),  
with which the current flow through the first LED cluster (40)  
can be monitored.

Q10 7. (Amended) The drive circuit as claimed in claim 1,  
characterized in that it also comprises an undervoltage detection  
device (64) which is designed to output an undervoltage warning  
signal (76) when the supply voltage ( $U_{Batt}$ ) falls below a  
prescribable value ( $U_{Ref1}$ ).

Q11 9. (Amended) The drive circuit as claimed in claim 7,  
characterized in that the prescribable value ( $U_{Ref1}$ ) can be set  
manually or can be prescribed permanently.

10. (Amended) The drive circuit as claimed in claim 3,  
characterized in that it also comprises an output unit (50, 50c,  
ST1) to which the information signal (78) and/or the undervoltage  
warning signal (76) can be transmitted.

12. (Amended) The drive circuit as claimed in claim 1,  
characterized in that it also comprises a closing delay device  
(74) which is designed to deactivate the output unit (50, 50c,  
ST1) for a predetermined time after the closure of the drive  
5 circuit.

Q12 13. (Amended) The drive circuit as claimed in claim 10,  
characterized in that the output unit (50, 50c, ST1) comprises a  
flip-flop (88), the base of the transistor (ST1) being connected  
to the output of the flip-flop (88), and the set input (S) of the  
5 flip-flop (88) being connected to the undervoltage detection  
device (64) in order to transmit the undervoltage warning signal

(76), and/or being connected to the comparison unit (50a) in order to transmit the information signal (78).

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5 14. (Amended) The drive circuit as claimed in claim 12, characterized in that the closing delay device (74) is designed to apply a closing delay signal (80) to the reset input (R) of the flip-flop (88) of the output unit (50, 50c, ST1) over the duration of the closing delay.

5 15. (Amended) The drive circuit as claimed in claim 1, characterized in that the actual magnitude ( $U_{\text{Mess}}$ ) corresponds to a time average value of the sum of the currents through at least two, in particular through all of the second LED clusters (42, 44).

Respectfully submitted,

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